REMARKS

Claims 2, 4-16 and 20-32 were pending in this application. Claims 6, 24 and 27 have been amended, and claims 33 and 34 have been added. Hence, claims 2, 4-16 and 20-34 are now pending. Reconsideration of the subject application as amended is respectfully requested.

Claims 6, 7, and 24-29 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 2, 4, 5, 7-16, 25 and 32, are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one of ordinary skill in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 2, 4, 5, 8, 9 and 32 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Grider et al.

Claim 10 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above.

Claims 11-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above.

Claims 6, 7 and 20-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above.

REJECTIONS UNDER 35 U.S.C. §112

Claims 6, 7, and 24-29 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. More specifically, the Office Action of 1/15/02 rejects claims 6, 24 and 27 because the term "substantially" is used. In response, the term "substantially" has been removed from each of the aforementioned claims. Hence, Applicant respectfully requests withdrawal of the rejection.

Claims 2, 4, 5, 7-16, 25 and 32, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one of ordinary skill in the art to which it pertains, or with which it is most nearly connected, to make

and/or use the invention. More specifically, the claims are rejected because the cited art, Grider et al., teaches a process that is distinct from that taught by Applicant's disclosure. Office Action of 1/15/02 at pp. 3-4. Such a basis for rejecting a claim is flawed for a variety of reasons.

For one, the affidavit provided herewith in accordance with 37 CFR 1.132 states that "[e]xperimental evidence verifies that adding a halogen, such as Flourine to a substrate at a concentration greater than approximately 1E14 per square centimeter *increases* oxide thickness at locations where the halogen is introduced." Affidavit at ¶3 (emphasis original). Further, the affidavit provides experimental data evidencing that the increase in oxide thickness verses the introduction of halogen containing impurities. Affidavit at ¶3 (citing Exhibit A attached thereto). Thus, when considered as a whole, the evidence supports a conclusion that one of ordinary skill in the art would have been able to make and use the inventions provided in the application at issue without undue experimentation as of the date of filing. Hence, Applicant respectfully requests withdrawal of the rejection.

Further, before rejecting a claim based on enablement, "[t]he examiner's analysis must consider all of the evidence related to each of the factors [set forth in MPEP §2164.01(a)], and any conclusion of non-enablement must be based on the evidence as a whole". MPEP at § 2164.01(a) citing In re Wands, 858 F.2d 737, 740, 8 USPQ2d 1401, 1407; see also, MPEP at §§ 2164.08, 2164.05(a), 2164.05(b), 2164.03, 2164.02, 2164.06. The Office Action does not suggest that such analysis was performed, and indeed does not even address whether the proper legal standard supporting a rejection of non-enablement has been met. Rather, without identifying any legal standard at all, the rejection simply makes a bald assertion that because Applicant's disclosure differs from the prior art, that it is somehow not enabled. As such, Applicant respectfully requests that the rejection be withdrawn for this additional reason.

REJECTIONS UNDER 35 U.S.C. §§ 102 and 103

Claims 2, 4, 5, 8, 9 and 32 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Grider et al. (U.S. Patent No. 6,093,659). Claims 10-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above. Claims 6, 7 and 20-31 have been rejected under 35 U.S.C. § 103(a) as being unpatentable

over Grider et al. as applied to claims 2, 4, 5, 8, 9 and 32 above. Applicant respectfully traverses the rejections with respect to independent claims 2, 6, 20, 24, 27 and 32.

Claims 2, 4, 5, 8, 9 and 32 are rejected as being anticipated by Grider et al. Applicant respectfully traverses the rejection first with respect to independent claim 2. which includes, *inter alia*, providing a substrate having first and second regions where the oxide layer at the first region is thicker than at the second region. The oxide layer at the first region is thicker than at the second region due to the halogen-containing impurities introduced into the first region. Thus, the halogen-containing impurities promote the oxide growth resulting in greater oxide thickness in the first region. Such a process is illustrated in Figure 2 of the present application.

At the outset, it should be noted that the Office Action asserts contradictory rejections. First, the Office Action asserts that Grider et al. teaches each and every limitation of Applicant's claims 2, 4, 5, 8, 9 and 32. Office Action of 1/15/02 at p2; see also, MPEP at §2131. Then, to support a flawed rejection based on 35 U.S.C. § 112, the same Office Action correctly notes that "Grider et al. teaches that increasing the halogen concentration results in decreasing the oxide thickness". Office Action of 1/15/02 at pp. 3-4 citing Grider et al. at col. 2, ll. 50-56. Thus, the rejection based on 35 U.S.C. § 102 is simply wrong in light of the acknowledgement in the Office Action that Grider et al. not only does not teach each element, but explicitly contradicts at least one element.

As noted by the Office Action, and in direct contrast to claim 2, Grider et al. discloses introduction of "halogen species, such as fluorine or chlorine, to *retard* oxidation." Grider at col. 1, ll. 65-67 (emphasis added); see also, col. 2, ll. 47-53. Thus, Grider et al. in fact teaches away from Applicant's invention as provide in claim 2. As Grider et al. does not disclose, teach or suggest a method whereby halogen-containing impurities are introduced to promote oxide growth, Grider et al. does not anticipate claim 2 as amended. Hence, at least because of the aforementioned limitation in claim 2, Applicant respectfully requests withdrawal of the rejection of claim 2 and allowance of claim 2 and all claims dependent therefrom. This include claims 2, 4, 5, 8-16.

Independent claims 20 and 32, as well as, dependent claims 7 and 25 include similar limitation to that discussed with reference to claim 2. For at least the reasons mentioned in relation to claim 2, applicant respectfully requests withdrawal of the rejections and allowance of these claims and all those that depend therefrom. This includes claims 7, 20-23, 25 and 30-32.

Claim 6 provides, *inter alia*, "providing a semiconductor substrate having a first semiconductor surface where a first oxide layer thickness is desired and a second semiconductor surface where a second oxide layer thickness is desired, wherein said first semiconductor surface is adjacent said second semiconductor surface". *The first semiconductor surface is located directly adjacent to the second semiconductor surface.*

Halogen-containing impurities are introduced into an exposed surface of the semiconductor substrate to form a higher halogen concentration in the first region as compared to the second region. An oxidizing process is performed on the semiconductor substrate to simultaneously form the first oxide layer thickness at the first semiconductor surface and the second oxide layer thickness at the second semiconductor surface. In this way, *the first and second oxide layer thicknesses are formed adjacent one another above the adjacent semiconductor surfaces.*

In contrast, Grider et al. discloses providing a substrate 30 having a first semiconductor surface area and a second semiconductor surface area separated by an isolation structure 32. See e.g., Grider et al. at Figs. 2-5; col. 2, ln. 62- col. 3, ln. 20.. As the two semiconductor surfaces of Grider et al. are explicitly separated by an isolation structure (32), Grider et al. does not disclose, teach or suggest two directly adjacent semiconductor surface areas as provided in Applicant's claim 2.

Accordingly, Grider et al. fails to disclose, teach or suggest every element of Applicant's claim 6. Hence, for at least this reason, Applicant respectfully requests withdrawal of the rejections to claim 6 and allowance thereof, as well as all claims dependent therefrom. This includes claims 6, 7 and 29.

Independent claims 24 and 27 each include limitations similar to that discussed with relation to claim 6. More specifically, among other elements:

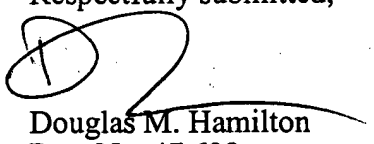
> Claim 24 provides, *inter alia*, "providing a semiconductor substrate having a first semiconductor surface area where a first oxide layer thickness is desired and a second semiconductor surface area where a second oxide layer thickness is desired, said first semiconductor surface area directly adjacent said second semiconductor surface area"; and
>
> Claim 27 provides, *inter alia*, "providing a semiconductor substrate having a first semiconductor surface area where a first oxide layer thickness is desired, a second semiconductor surface area where a second oxide layer thickness is desired, and a third semiconductor surface area where a third oxide layer thickness is desired, wherein said first and second semiconductor surface areas are contiguous";

Thus, for at least the aforementioned reason, independent claims 24 and 27, as well as those that depend therefrom, are also in condition for allowance. This includes claims 24-28. Further, the added claims 33 and 34 are allowable for one or more of the aforementioned reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 303-571-4000.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

2. (Previously Thrice Amended) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, wherein said first oxide layer thickness is greater than said second oxide layer thickness;

introducing halogen-containing impurities into an exposed surface of said semiconductor substrate to form a higher halogen concentration in said first region than in said second region;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region; and

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

4. (Previously Amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises an ion implantation.

5. (Previously Amended) The method of claim 2 wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. (Six Times Amended Herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first semiconductor surface where a first oxide layer thickness is desired and a second semiconductor surface where a second oxide layer thickness is desired, wherein said first semiconductor surface is adjacent said second semiconductor surface;

introducing halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said semiconductor substrate **[substantially]** below said first

semiconductor surface than in said semiconductor substrate **[substantially]** below said second semiconductor surface;

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness disposed above said first semiconductor surface and said second oxide layer thickness disposed above said second semiconductor surface; and

wherein introducing said halogen-containing impurities comprises introducing halogen-containing impurities into said semiconductor substrate **[substantially]** below said first semiconductor surface at a first concentration and introducing halogen-containing impurities into said semiconductor substrate **[substantially]** below said second semiconductor surface at a second concentration, said first concentration greater than said second concentration, both said first and second concentrations formed of a dosage of said halogen-containing impurities greater than about 1 x 10^{14} carriers/cm^2 and less than about 1 x 10^{15} carriers/cm^2.

7. (Previously Amended) The method of claim 6 wherein said halogen-containing impurities promote oxide growth on said semiconductor substrate such that said first oxide layer thickness is greater than said second oxide layer thickness.

8. (Previously Amended) The method of claim 2 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

9. (Previously Amended) The method of claim 2 wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein introducing said halogen-containing impurities also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region and in said second region.

10. (Previously Amended) The method of claim 2 wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. (As filed) The method of claim 11 wherein said first memory gate electrode is part of a split gate cell.

14. (As filed) The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. (As filed) The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

20. (Previously Four Times Amended) A method of forming a semiconductor integrated circuit, said method comprising:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities through said gate dielectric layer and into said second region; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region by an oxidizing process, wherein said halogen-containing impurities in said second region promote formation of said second thickness of dielectric material.

21. (Previously Three Times Amended) The method of claim 20

wherein said selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region, said halogen-

containing impurities in said second region formed of a dosage greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2

22. (As filed) The method of claim 20 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23. (As filed) The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

24. (Thrice Amended Herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first semiconductor surface area where a first oxide layer thickness is desired and a second semiconductor surface area where a second oxide layer thickness is desired, said first semiconductor surface area directly adjacent said second semiconductor surface area;

forming a dielectric layer on said substrate;

masking said dielectric layer to expose said first semiconductor surface area;

introducing halogen-containing impurities through said dielectric layer and into said semiconductor substrate to form a higher halogen concentration in a volume of said semiconductor substrate **[substantially]** below said first semiconductor surface area than in a volume of said semiconductor substrate **[substantially]** below said second semiconductor surface area; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first semiconductor surface area and said second oxide layer thickness at said second semiconductor surface area;

said oxidizing process comprising a thermal anneal at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

25. (Previously Added) The method of claim 24 wherein said halogen-containing impurities promote oxide growth on said semiconductor substrate such that said first oxide layer thickness is greater than said second oxide layer thickness.

26. (Previously Added) The method of claim 24 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

27. (Four Times Amended Herein) A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first semiconductor surface area where a first oxide layer thickness is desired, a second semiconductor surface area where a second oxide layer thickness is desired, and a third semiconductor surface area where a third oxide layer thickness is desired, wherein said first and second semiconductor surface areas are contiguous;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in a first volume of said semiconductor substrate **[substantially]** below said first semiconductor surface area than in a second volume of said semiconductor substrate **[substantially]** below said second semiconductor surface area, and a different halogen concentration in a third volume of said semiconductor substrate **[substantially]** below said third semiconductor surface area than in said first volume and said second volume, each of said higher halogen concentration and said different halogen concentration; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first semiconductor surface area and said second oxide layer thickness at said second semiconductor surface area.

28. (Previously Once Amended) The method of claim 27 wherein said performing an oxidizing process also simultaneously forms said third oxide layer thickness at said third semiconductor surface area.

29. (Previously Once Amended) The method of claim 6 wherein at least one of said first and second concentrations formed of a dosage of said halogen-containing impurities greater than about 1×10^{14} carriers/cm^2 and less than about 1×10^{15} carriers/cm^2.

30. (Previously Added)The method of claim 20 wherein said forming said first and second thickness of dielectric material comprises an anneal process performed at about 780 to about 1000 degrees Celsius, and for a duration of about ten (10) minutes to about five (5) hours.

31. (Previously Added) The method of claim 30 wherein said anneal process is further performed at a pressure of about 760 Torr.

32. (Previously Once Amended) A method of forming a semiconductor device, the method comprising:

providing a substrate having a first region and a second region;

introducing halogen-containing impurities into the substrate to form a higher concentration in the first region than in the second region;

placing the substrate in an oxidizing environment, wherein a thicker oxide layer forms over the first region where the halogen-containing impurities are located than over the second region;

in a single step, forming a conductive layer disposed above the first region and the second region; and

removing portions of the oxide layer and the conductive layer to form gate structures disposed over the substrate.

--33. (Added Herein) A method of forming a semiconductor device, the method comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, wherein said first oxide layer thickness is greater than said second oxide layer thickness;

introducing flourine impurities into an exposed surface of said semiconductor substrate to form a higher flourine concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

34. (Added Herein) A method of forming a semiconductor device, the method comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, wherein said first oxide layer thickness is greater than said second oxide layer thickness;

introducing halogen impurities into an exposed surface of said semiconductor substrate to form a higher halogen concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.--